IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Mericas**

Serial No.: **09/310,912**

Filed: **May 13, 1999**

For: **Method and System for Counting Non-Speculative Events in a Speculative Processor**

§ Group Art Unit: **2124**
§
§ Examiner: **Chavis, John Q.**
§
§ Attorney Docket No.: **AT9-99-073**
§

Certificate of Mailing Under 37 C.F.R. § 1.8(a)
I hereby certify this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on December 18, 2002.

By: Dell Whitton
Dell Whitton

TRANSMITTAL DOCUMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:
ENCLOSED HEREWITH:

- Reply Brief (in triplicate); and
- Our return postcard.

No fees are believed to be required. If, however, any fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to IBM Corporation Deposit Account No. 09-0447.

Respectfully submitted,

Duke W. Yee
Registration No. 34,285
CARSTENS, YEE & CAHOON, LLP
P.O. Box 802334
Dallas, Texas 75380
(972) 367-2001
ATTORNEY FOR APPLICANT

Docket No. AT9-99-073 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Mericas** §
§ Group Art Unit: **2124**
Serial No. **09/310,912** §
§ Examiner: **Chavis, John Q.**
Filed: **May 13, 1999** §
§
For: **Method and System for Counting Non-Speculative Events in a Speculative Processor** §
§

Assistant Commissioner for Patents
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

Certificate of Mailing Under 37 C.F.R. § 1.8(a)
I hereby certify this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on December 18, 2002.

By: Dell Whitton
Dell Whitton

REPLY BRIEF

This Reply Brief is in response to the Examiner's Answer, dated November 5, 2002.

Any fees required under § 1.17(c), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF REPLY BRIEF.

This brief is transmitted in triplicate. (37 C.F.R. 1.192(a))

SUMMARY OF INVENTION

The Examiner's Answer indicates that the Summary of Invention section of the Appeal Brief is deficient, because the summary includes features which are not claimed. More particularly, the Examiner's Answer objects to the mention of "predicting the outcome of conditional branches of certain instructions before the data on which the certain instructions depend is available," a feature which is fundamental to speculative processors. The Examiner is apparently unwilling to acknowledge the existence or knowledge of speculative processors in the art. Appellant respectfully disagrees. However, to simplify the issues, please replace the Summary of Invention in the Appeal Brief with the following:

> The present invention provides a performance monitor for a speculative processor. See specification, page 10, lines 8-28. The performance monitor includes performance monitor counters. See specification, page 8, lines 18-26. The performance monitor may include one or more interim counters that hold the count of occurrences for monitored events that are caused by instructions that may never complete. See specification, page 16, line 19, to page 17, line 7. When an instruction completes, the contents of the completed instruction's interim counter is added to a performance monitor counter. See page 17, lines 8-23. The present invention may also compute a difference between performance monitor counters and interim counts to generate a count of events related to speculatively executed instructions. See page 20, line 29, to page 21, line 6.

GROUPING OF CLAIMS

The Examiner's Answer states that claims 1-17 stand or fall together because Appellant's brief does not include reasons in support of the groupings in the Appeal Brief. Appellant respectfully disagrees. 37 CFR 1.192(c)(7), as cited by the Examiner's Answer, states:

> (7) Grouping of claims. For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

Paragraph (c)(8) in 37 CFR 1.192 describes the Argument section of the Appeal Brief. Clearly, the claims should stand or fall in at least two groups, because there are two grounds of rejection in the

Final Office Action.

However, the Appeal Brief does indeed contain a statement that the claims do not stand or fall together and arguments in the Argument section of the Appeal Brief explaining why the claims are believed to be separately patentable. Group A, claims 1, 12, and 16, is argued as being separately patentable on page 4, line 2, to page 8, line 16. Group B, claim 4, is argued as being separately patentable on page 4, lines 17-27. Group C, claims 6, 15, and 17, is argued as being separately patentable on page 8, line 28, to page 9, line 11. Claims 15 and 17 stand or fall with claim 6. Group D, claim 7, is argued as being separately patentable on page 9, lines 12-29. Group E, claims 3 and 14, is argued as being separately patentable on page 9, line 30, to page 10, line 10. Claim 14 stands or falls with claim 3. Group F, claim 8, is argued as being separately patentable on page 10, lines 11-13. Group G, claim 9, is argued as being separately patentable on page 10, lines 13-14. Group H, claim 10 is argued as being separately patentable on page 10, lines 13-18. Group I, claims 2, 5, 11, and 13, is argued as being separately patentable on page 11, line 1, to page 12, line 20.

Therefore, Appellant maintains that the claims should be grouped into the groups set forth in the Appeal Brief.

ARGUMENT

The Examiner's Answer states:

> In reference to the 35 USC 102(e) rejection referenced above in item 10, the applicant rehashes arguments presented in the final rejection. That is, he indicates that his system monitors events that occur during the execution of instructions by a speculative processor, generates a count of occurrences of the events for all instructions executed by the speculative processor and generates a count of occurrences of the events for instructions completed by the speculative processor. Then, he goes on to define a speculative processor. He indicates that a speculative processor is a modern processor that **may** speculatively execute instructions that **may** be cancelled or flushed without completely executing because the condition for which they were speculatively executed did not occur. Again, it is not clear (1) where this feature is in the claims, as indicated above; or (2) how this is different from Dollins event processor (figure 1, items 12 and 14 and col. 5 line 41-46). The applicant makes multiple references to the specifications (for example, on page 5, 1st complete paragraph, he refers to page 3 lines 1-6) for support for his claimed invention, this makes it appear that the specifications (instead of the claims is being argued over the cited reference. A standard processor is considered to provide for execution of event (occurrences that may or may not be satisfied) functions or

> programs and canceling the functions or programs if the event being monitored does not occur (i.e. "discarding events", col. 5 lines 4-7) to free up space being utilized. Thus, Dollin's processors indeed are also considered to provide for this feature.

Examiner's Answer, dated November 5, 2002. Appellant respectfully disagrees. It is certainly clear where the feature of a speculative processor is in the claims, because the feature appears in the claims numerous times. Appellants submit that there is nothing unclear about a feature that is expressly recited numerous times in each and every independent claim.

Furthermore, the Examiner's Answer wonders how a speculative processor is different from the processor of Dollin. This difference is certainly clear to a person of ordinary skill in the art. Dollin simply does not teach a processor that speculatively executes instructions. Again, Appellants submit that there is nothing unclear about a feature that is expressly recited in the claims, but found nowhere in the applied reference.

Appellant refers to the specification for a definition of "speculative processor" only because the Examiner is apparently unwilling to recognize this feature. Appellant submits that a definition is unnecessary, since a person of ordinary skill in the art would readily acknowledge that a speculative processor is not just any standard processor. However, when provided with a definition from the specification, the Examiner dismisses the feature of a "speculative processor" as not being claimed, despite the feature appearing numerous times in each and every independent claim.

The Examiner's answer then argues that a standard processor is somehow considered to provide for execution of event functions or programs and canceling the functions or programs if the event is discarded to free up space. Appellant submits that an event that is discarded to free up space is not an event that does not occur. Furthermore, there is an unavoidable difference between events that occur in a network, as in Dollin, and events that occur in a speculative processor, as in the present invention.

The Examiner's Answer also states:

> The applicant further appears to indicate that Dollin does not provide a processor (page 5, second complete paragraph); however, see again the references above. Furthermore, the processors are considered to provide for each of the features claimed. Then, he indicates that Dollin provides processors 12 and 14, as indicated above. The applicant's statements on page 6 (first complete paragraph) are then sufficient to indicate that Dollin provides processors and as indicated above the processors provide for the applicant's definition of speculative features, as indicated above; although the features are not apparent in the claims.

Examiner's Answer, dated November 5, 2002. Appellant has recognized over and over that Dollin teaches processors. However, the processors of Dollin are not speculative processors. Furthermore, Dollin does not teach or suggest the actual method steps that are performed in the context of a data processing system comprising a speculative processor, as recited in representative claim 1.

The Examiner's Answer then states:

> Then, the applicant continues to argue the definition of "speculative processors", which is not supported by the claims. Therefore, no further discussion on this matter is deemed necessary; since, the applicant merely mentions the term and provides no support in the claims to indicate anything other than standard feature provided for by any general processor exist. The applicant further indicates that Dollin does not teach or suggest associating events with instructions executed by a speculative processor; while Dollin's "determining, comparing, discarding, comparing" are all instructions, associated with events (counting of lost, inserted and corrupted functions) executed by his processor (which inherently, based on the characteristic or functionality of events, may or may not completely execute instructions when the event does not occur). Furthermore, again, the applicant appears to stretch his argument in an attempt to incorporate the specifications in the claims. An example of this is illustrated via the applicant's argument about "flushing an event", which is not specified in the claims.

Examiner's Answer, dated November 5, 2002. The claims are to be interpreted in light of the specification. *In re Okuzawa*, 537 F.2d 545, 190 U.S.P.Q. 464 (C.C.P.A. 1976). According to M.P.E.P.:

> The meaning of every term used in any of the claims should be apparent from the descriptive portion of the specification with clear disclosure as to its import.... A term used in the claims may be given a special meaning in the description.

M.P.E.P. § 608.01(o). It is not the role of the claims to enable one skilled in the art to reproduce the invention, but rather to define the legal metes and bounds of the invention. *In re Rainer*, 305 F.2d 505, 134 U.S.P.Q. 343 (C.C.P.A. 1962); *In re Anderson*, 471 F.2d 1237, 176 U.S.P.Q. 331 (C.C.P.A. 1973); and *In re Mercier*, 515 F.2d 1161, 185 U.S.P.Q. 774 (C.C.P.A. 1975). Appellant submits that the limitation of a "speculative processor" is clearly and unavoidably recited in each and every independent claim. A definition of the term is not necessary, since the term "speculative processor" is easily recognized and understood by a person of ordinary skill in the art. However, the term is also defined in the specification to aid a layperson in understanding

the claimed features. Therefore, the Examiner cannot dismiss the limitation or the definition for the disputed feature as not being present in the claims.

The Examiner also attempts to stretch the teachings of Dollin so that monitoring of events in a network is somehow equivalent to monitoring of events within a speculative processor. Appellant respectfully disagrees. Dollin is not concerned with a speculative processor. Therefore, Dollin does not disclose the context in which the present invention operates or the specific steps, means, or instructions recited in the claims.

The Examiner's Answer further states:

> Moreover, the applicant indicates that no analysis has been presented to indicate why Dollin's "inserted events" are equivalent to occurrences of the specified event for instructions completely executed. While, it is clear that "inserted events" are "all instructions that are executed by Dollin's processor" in order for monitoring to occur to determine if the event criteria has been satisfied, col. 8 lines 35-45. He further indicates that "corrupted events" does not provide an indication of instructions that are completely executed. However, the feature is inherent to determine the quality of service.

Examiner's Answer, dated November 5, 2002. The cited portion of Dollin makes no mention whatsoever of "generating a count of occurrences of the specified event for all instructions executed by the speculative processor," as recited in representative claim 1. Certainly, it is not clear that "inserted events" are related in any way to the present invention, because Dollin has nothing whatsoever to do with speculative processors. Furthermore, while monitoring for "corrupted events" may be inherent to determining quality of service for a network, this teaching has nothing to do with the present invention.

The Examiner's Answer states:

> The applicant further argues that Dollin does not teach associating an interim counter with a particular; while again, the quality of service feature which generates reports based on "all instructions", "completed instructions" and "lost" or "failed instructions", (Dollin) col. 5 lines 47-55 and col. 12 lines 3-8, clearly provides for the feature. In reference to the applicant's discussion of claim 6, see again the discussion above. That is, differences are inherently calculated to determine "quality of service".

Examiner's Answer, dated November 5, 2002. Appellant respectfully disagrees. The cited portion makes no mention whatsoever of "all instructions," "completed instructions," or "lost" or "failed instructions." The Examiner appears to point to arbitrary portions of the applied prior art

and concludes that the claim limitations are "clearly" provided. To the contrary, Dollin has nothing to do with speculative processors and clearly fails to teach or suggest "reading from a first counter a count of occurrences of a specified event for all instructions executed by the speculative processor," "reading from a second counter a count of occurrences of the specified event for instructions completely executed by the speculative processor," and "computing a difference between the count of occurrences of the specified event for all instructions and the count of occurrences of the specified event for all completed instructions as a count of occurrences of the specified event for instructions speculatively executed by the speculative processor," as recited in claim 6. Since the applied art fails to teach or suggest each and every claim limitation, claim 6 is not anticipated by Dollin. Therefore, the Examiner's Answer does not establish a *prima facie* case of anticipation for claim 6 and the rejection should be withdrawn.

The Examiner's Answer also states:

> In reference to claim 7, note in the abstract that "whenever an event is detected, an event report is generated". Therefore, Dollin is considered to utilize a first counter (whenever an event is detected, see the abstract and the (Quality of Service) QOS unit in col. 11 lines 61-col. 12 line 8) and a second counter (to indicate when a match does not occur) and the third counter for keeping a count of the completed matches to enable efficient report generation and specifying QOS as is known in the art, as a percentage of matches completed over the total to determine performance (QOS).

Examiner's Answer, dated November 5, 2002. Appellant respectfully disagrees. Dollin simply does not teach or suggest incrementing a first counter and a second counter in response to detecting an occurrence of a particular specified event and adding the second counter to a third counter in response to detecting a completion of an instruction, as recited in claim 7. By whom is Dollin considered to utilize a first counter, a second counter, and a third counter? Neither the cited portion nor any other portion of Dollin teaches or suggests these features. Since the applied art fails to teach or suggest each and every claim limitation, claim 7 is not anticipated by Dollin. Therefore, the Examiner's Answer does not establish a *prima facie* case of anticipation for claim 7 and the rejection should be withdrawn.

The Examiner's Answer further states:

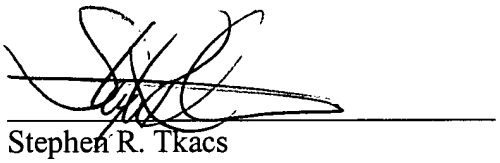
> The features of monitoring a plurality of events (claims 3, 8-10 and 14) are taught via Dollin in col. 11 lines 5-14. The applicant further claims that Dollin does not teach monitoring a plurality of specified events for each instruction executed by the speculative processor. The applicant should note that Dollin's

> event monitoring is inherently for each instruction executed to ensure that the desired instruction (specified event) is not overlooked because again it has to be evaluated to determine if the event is satisfied, col. 8 lines 35-45. Furthermore, Dollin's entire monitoring process occurs at one (the receiver, i.e. within a data processing system) of the processors for each instruction executed, see the abstract. In other words, in Dollin's system, each instruction executed (per specified event) must have been monitored accordingly to ensure that the desired instruction has not been overlooked.

Examiner's Answer, dated November 5, 2002. Appellant respectfully disagrees. The applied reference has nothing to do with monitoring for completion of instructions in a speculative processor. Dollin teaches a method and apparatus for making quality of service measurements on a connection across a network. The apparatus of Dollin tracks events in existing traffic carried by a connection of interest. See col. 3, lines 16-19. In other words, the apparatus and method of Dollin monitors for events in data units transmitted across the connection of interest. Dollin teaches generating counts of lost, inserted, and corrupted events for the connection. See col. 4, line 48, to col. 5, line 39. However, the network event monitoring of Dollin is not equivalent to the present invention. The Examiner's Answer describes the network traffic events as "instructions" in an attempt to make the otherwise non-analogous teachings seem somewhat similar to the claimed invention. To the contrary, Dollin is not concerned with a speculative processor; therefore, Dollin does not disclose the context in which the present invention operates or the specific steps, means, or instructions recited in the claims.

CONCLUSION

In view of the above, Appellant respectfully submits that the rejections of claims 1-17 are overcome. Accordingly, it is respectfully urged that the Examiner's rejections of claims 1-17 not be sustained.



Stephen R. Tkacs
Reg. No. 46,430
Carstens, Yee & Cahoon, LLP
PO Box 802334
Dallas, TX 75380
(972) 367-2001